2 Ω CMOS ±5 V/5 V, SPST Switches

ADG601/ADG602

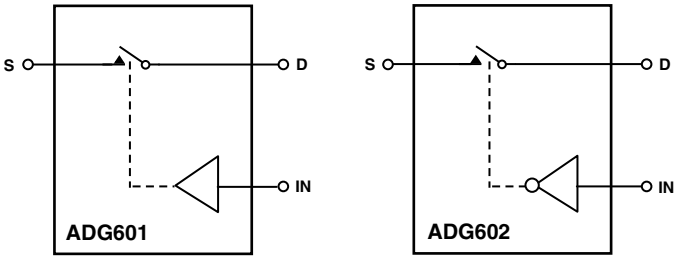
FEATURES

Low On Resistance 2.5 Ω Max
<0.6 Ω On Resistance Flatness
Dual ±2.7 V to ±5.5 V or Single 2.7 V to 5.5 V Supplies
Rail-to-Rail Input Signal Range
Tiny 6-Lead SOT-23 and 8-Lead Micro-SOIC Packages
Low Power Consumption
TTL/CMOS-Compatible Inputs

APPLICATIONS

Automatic Test Equipment
Power Routing
Communication Systems
Data Acquisition Systems
Sample and Hold Systems
Avionics
Relay Replacement
Battery-Powered Systems

FUNCTIONAL BLOCK DIAGRAMS



SWITCHES SHOWN FOR A LOGIC "1" INPUT

GENERAL DESCRIPTION

The ADG601/ADG602 are monolithic CMOS SPST (Single Pole, Single Throw) switches with On Resistance typically less than 2.5 Ω. The Low On Resistance flatness makes the ADG601/ADG602 ideally suited to many applications, particularly those requiring low distortion. These switches are ideal for replacements for mechanical relays because they are more reliable, have lower power requirements, and package size is much smaller.

The ADG601 is a normally open (NO) switch, while the ADG602 is normally closed (NC). Each switch conducts equally well in both directions when ON, with the input signal range extending to the supply rails.

They are available in tiny 6-lead SOT-23 and 8-lead Micro-SOIC packages.

Table I. Truth Table

ADG601 In	ADG602 In	Switch Condition
0	1	OFF
1	0	ON

PRODUCT HIGHLIGHTS

1. Low On Resistance (2 Ω typical)
2. Dual ±2.7 V to ±5.5 V or Single 2.7 V to 5.5 V Supplies
3. Tiny 6-lead SOT-23 and 8-lead Micro-SOIC Packages
4. Rail-to-Rail Input Signal Range

REV. 0

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Tel: 781/329-4700 **www.analog.com**
Fax: 781/326-8703

ADG601/ADG602–SPECIFICATIONS

DUAL SUPPLY (V_{DD} = 5 V ± 10%, V_{SS} = –5 V ± 10%, GND = 0 V, unless otherwise noted.)

Parameter	B Version 25°C	B Version –40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		V_{SS} to V_{DD}	V	
				V_{DD} = +4.5 V, V_{SS} = –4.5 V
On Resistance (R_{ON})	2		Ω typ	V_S = ±4.5 V, I_S = –10 mA;
	2.5	5.5	Ω max	Test Circuit 1
On-Resistance Flatness ($R_{FLAT(ON)}$)	0.35		Ω typ	V_S = ±3.3 V, I_S = –10 mA
	0.4	0.6	Ω max	
LEAKAGE CURRENTS				
				V_{DD} = +5.5 V, V_{SS} = –5.5 V
Source OFF Leakage I_S (OFF)	±0.01		nA typ	V_S = +4.5 V/–4.5 V, V_D = –4.5 V/+4.5 V;
	±0.25	±1	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.01		nA typ	V_S = +4.5 V/–4.5 V, V_D = –4.5 V/+4.5 V;
	±0.25	±1	nA max	Test Circuit 2
Channel ON Leakage I_D, I_S (ON)	±0.01		nA typ	V_S = V_D = +4.5 V, or –4.5 V;
	±0.25	±1	nA max	Test Circuit 3
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4		V min
Input Low Voltage, V_{INL}		0.8		V max
Input Current				
I_{INL} or I_{INH}	0.005		μA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	μA max	
C_{IN}, Digital Input Capacitance	2		pF typ	
DYNAMIC CHARACTERISTICS[2]				
t_{ON}	80		ns typ	R_L = 300 Ω, C_L = 35 pF
	120	155	ns max	V_S = 3.3 V; Test Circuit 4
t_{OFF}	45		ns typ	R_L = 300 Ω, C_L = 35 pF
	75	90	ns max	V_S = 3.3 V; Test Circuit 4
Charge Injection	250		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; Test Circuit 5
Off Isolation	–60		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 6
Bandwidth –3 dB	180		MHz typ	R_L = 50 Ω, C_L = 5 pF; Test Circuit 7
C_S (OFF)	50		pF typ	f = 1 MHz
C_D (OFF)	50		pF typ	f = 1 MHz
C_D, C_S (ON)	145		pF typ	f = 1 MHz
POWER REQUIREMENTS				
				V_{DD} = +5.5 V, V_{SS} = –5.5 V
I_{DD}	0.001		μA typ	Digital Inputs = 0 V or 5.5 V
		1.0	μA max	
I_{SS}	0.001		μA typ	Digital Inputs = 0 V or 5.5 V
		1.0	μA max	

NOTES
[1]Temperature range is as follows: B Version: –40°C to +85°C.
[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

SINGLE SUPPLY[1] (V_{DD} = 5 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.)

Parameter	B Version 25°C	B Version –40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 V to V_{DD}	V	
				V_{DD} = 4.5 V
On Resistance (R_{ON})	3.5		Ω typ	V_S = 0 V to 4.5 V, I_S = –10 mA;
	5	8	Ω max	Test Circuit 1
On-Resistance Flatness ($R_{FLAT(ON)}$)	0.2	0.2	Ω typ	V_S = 1.5 V to 3.3 V, I_S = –10 mA
		0.35	Ω max	
LEAKAGE CURRENTS				
				V_{DD} = 5.5 V
Source OFF Leakage I_S (OFF)	±0.01		nA typ	V_S = 4.5 V/1 V, V_D = 1 V/4.5 V;
	±0.25	±1	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.01		nA typ	V_S = 4.5 V/1 V, V_D = 1 V/4.5 V;
	±0.25	±1	nA max	Test Circuit 2
Channel ON Leakage I_D, I_S (ON)	±0.01		nA typ	V_S = V_D = 4.5 V, or 1 V;
	±0.25	±1	nA max	Test Circuit 3
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current				
I_{INL} or I_{INH}	0.005		µA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	µA max	
C_{IN}, Digital Input Capacitance	2		pF typ	
DYNAMIC CHARACTERISTICS[2]				
t_{ON}	110		ns typ	R_L = 300 Ω, C_L = 35 pF
	220	280	ns max	V_S = 3.3 V; Test Circuit 4
t_{OFF}	50		ns typ	R_L = 300 Ω, C_L = 35 pF
	80	110	ns max	V_S = 3.3 V; Test Circuit 4
Charge Injection	20		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF, Test Circuit 5
Off Isolation	–60		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, Test Circuit 6
Bandwidth –3 dB	180		MHz typ	R_L = 50 Ω, C_L = 5 pF, Test Circuit 7
C_S (OFF)	50		pF typ	f = 1 MHz
C_D (OFF)	50		pF typ	f = 1 MHz
C_D, C_S (ON)	145		pF typ	f = 1 MHz
POWER REQUIREMENTS				
				V_{DD} = 5.5 V
I_{DD}	0.001		µA typ	Digital Inputs = 0 V or 5.5 V
		1.0	µA max	

NOTES
[1]Temperature range is as follows: B Version: –40°C to +85°C.
[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = 25°C unless otherwise noted)

V_{DD} to V_{SS} . . . . . 13 V
V_{DD} to GND . . . . . –0.3 V to +6.5 V
V_{SS} to GND . . . . . +0.3 V to –6.5 V
Analog Inputs[2] . . . . . V_{SS} –0.3 V to V_{DD} +0.3 V
Digital Inputs[2] . . . . . –0.3 V to V_{DD} +0.3 V
or 30 mA, whichever occurs first
Continuous Current, S or D . . . . . 100 mA
Peak Current, S or D
(Pulsed at 1 ms, 10% Duty Cycle Max) . . . . . 200 mA
Operating Temperature Range
Industrial (B Version) . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature . . . . . 150°C
Micro-SOIC Package
θ_{JA} Thermal Impedance . . . . . 206°C/W
θ_{JC} Thermal Impedance . . . . . 44°C/W
SOT_23 Package
θ_{JA} Thermal Impedance . . . . . 229.6°C/W
θ_{JC} Thermal Impedance . . . . . 91.99°C/W
Lead Temperature, Soldering (10 seconds) . . . . . 300°C
IR Reflow, Peak Temperature . . . . . 220°C

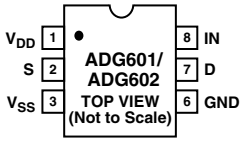
NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

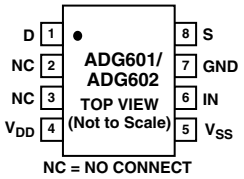
[2]Overvoltages at IN, S, or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

PIN CONFIGURATIONS

6-Lead Plastic Surface Mount (SOT_23)
(RT-6)



8-Lead Small Outline Micro-SOIC
(RM-8)



ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding Information*
ADG601BRT	–40°C to +85°C	Plastic Surface-Mount (SOT_23)	RT-6	STB
ADG601BRM	–40°C to +85°C	Micro Small Outline (Micro-SOIC)	RM-8	STB
ADG602BRT	–40°C to +85°C	Plastic Surface-Mount (SOT_23)	RT-6	SUB
ADG602BRM	–40°C to +85°C	Micro Small Outline (Micro-SOIC)	RM-8	SUB

*Branding on SOT_23 and Micro-SOIC packages is limited to three characters due to space constraints.

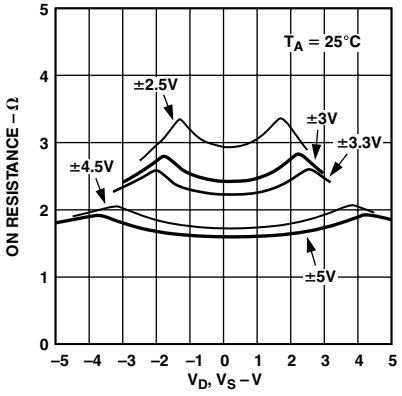
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG601/ADG602 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

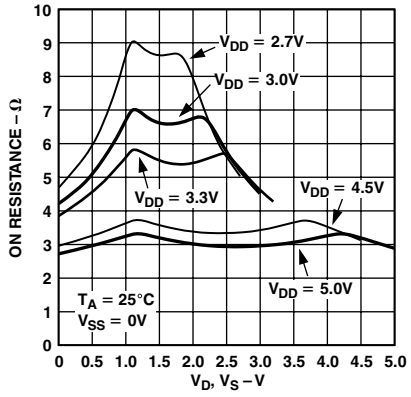
TERMINOLOGY

V_{DD}	Most Positive Power Supply Potential
V_{SS}	Most Negative Power Supply Potential
I_{DD}	Positive Supply Current
I_{SS}	Negative Supply Current
GND	Ground (0 V) Reference
S	Source Terminal. May be an input or output.
D	Drain Terminal. May be an input or output.
IN	Logic Control Input
V_D (V_S)	Analog Voltage on Terminals D, S
R_{ON}	Ohmic Resistance Between D and S
$R_{FLAT(ON)}$	Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.
I_S (OFF)	Source Leakage Current with the Switch "OFF"
I_D (OFF)	Drain Leakage Current with the Switch "OFF"
I_D, I_S (ON)	Channel Leakage Current with the Switch "ON"
V_{INL}	Maximum Input Voltage for Logic "0"
V_{INH}	Minimum Input Voltage for Logic "1"
$I_{INL}(I_{INH})$	Input Current of the Digital Input
C_S (OFF)	"OFF" Switch Source Capacitance. Measured with reference to ground.
C_D (OFF)	"OFF" Switch Drain Capacitance. Measured with reference to ground.
C_D,C_S(ON)	"ON" Switch Capacitance. Measured with reference to ground.
C_{IN}	Digital Input Capacitance
t_{ON}	Delay Between Applying the Digital Control Input and the Output Switching On.
t_{OFF}	Delay Between Applying the Digital Control Input and the Output Switching Off.
Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.
Off Isolation	A measure of unwanted signal coupling through an "OFF" Switch.
On Response	Frequency Response of the "ON" Switch
Insertion Loss	Loss Due to the ON Resistance of the Switch

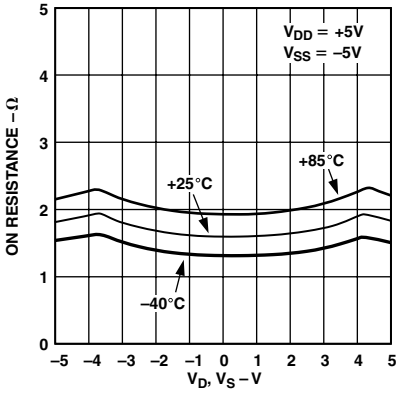
Typical Performance Characteristics



TPC 1. On Resistance vs. $V_D(V_S)$ (Dual Supply)

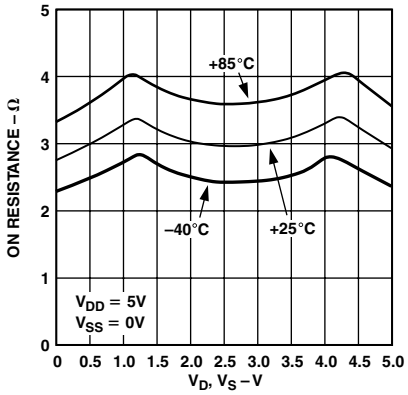


TPC 2. On Resistance vs. $V_D(V_S)$ (Single Supply)

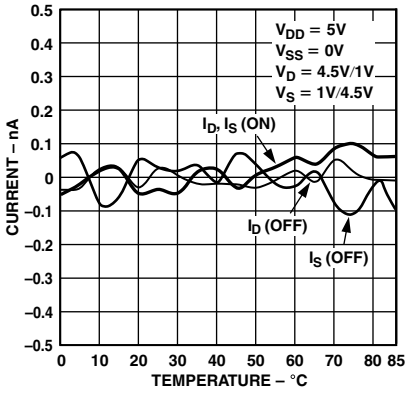


TPC 3. On Resistance vs. $V_D(V_S)$ for Different Temperatures (Dual Supply)

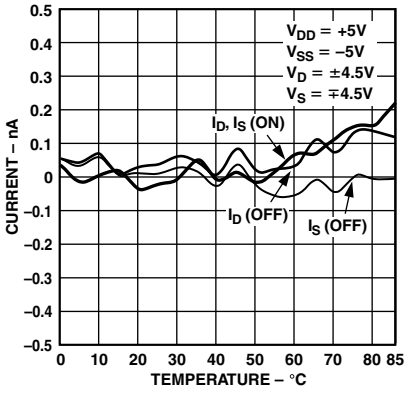
ADG601/ADG602–Typical Performance Characteristics (continued)



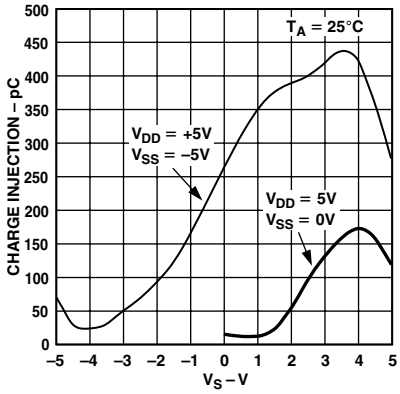
TPC 4. On Resistance vs. $V_D(V_S)$ for Different Temperatures (Single Supply)



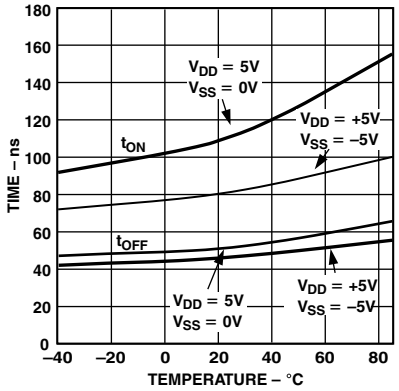
TPC 5. Leakage Currents vs. Temperature (Single Supply)



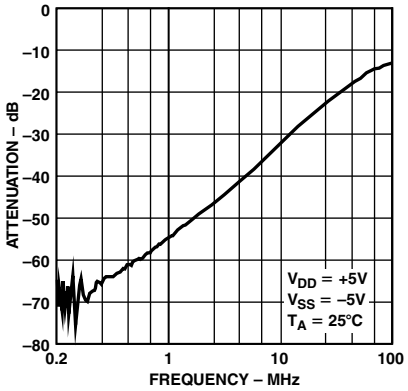
TPC 6. Leakage Currents vs. Temperature (Dual Supply)



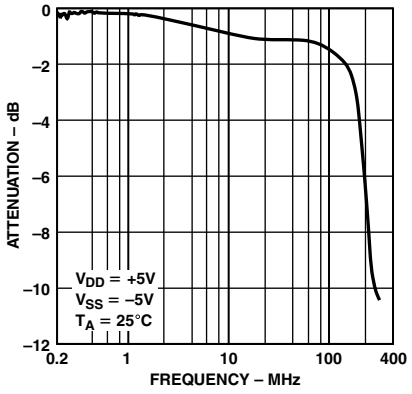
TPC 7. Charge Injection vs. Source Voltage



TPC 8. t_{ON}/t_{OFF} Times vs. Temperature

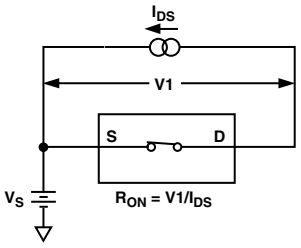


TPC 9. Off Isolation vs. Frequency

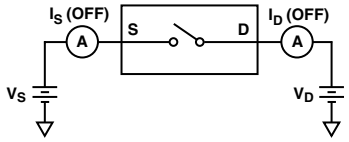


TPC 10. On Response vs. Frequency

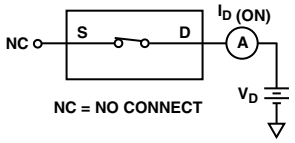
TEST CIRCUITS



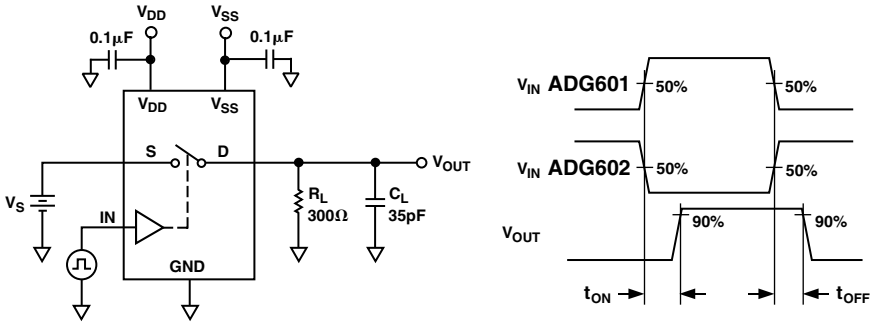
Test Circuit 1. On Resistance



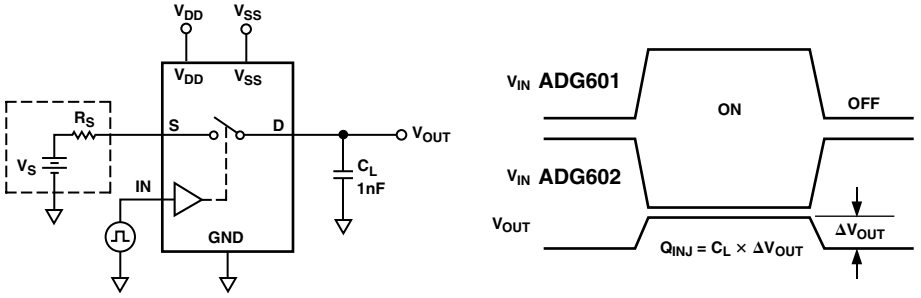
Test Circuit 2. Off Leakage



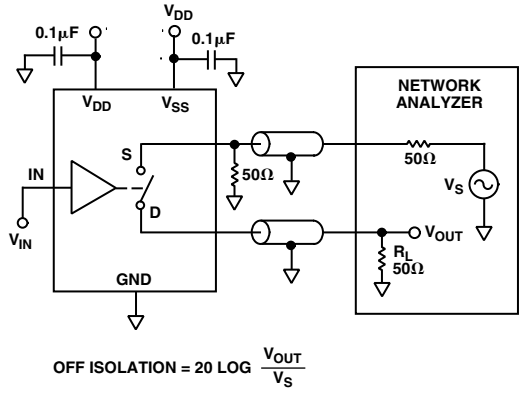
Test Circuit 3. On Leakage



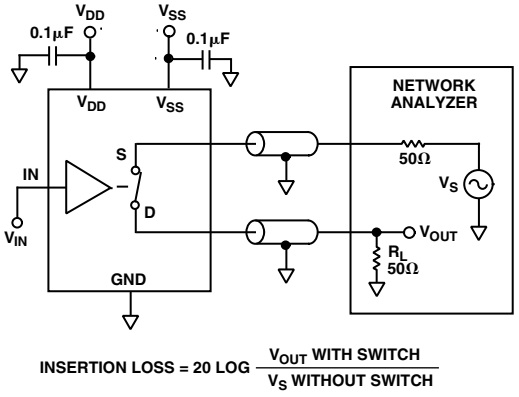
Test Circuit 4. Switching Times



Test Circuit 5. Charge Injection



Test Circuit 6. Off Isolation

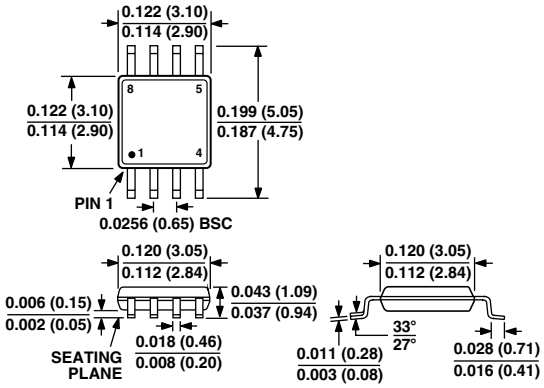


Test Circuit 7. Bandwidth

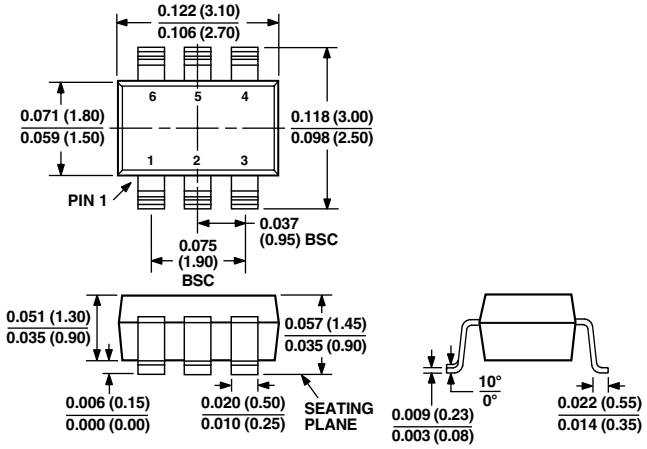
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead Micro-SOIC
(RM-8)



6-Lead Plastic Mount SOT-23
(RT-6)



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